WHAT IS CLAIMED IS:

1. An encoder comprising:

an information sequence generating means for generating a first information sequence by inserting a first DC control bit into an input information sequence at predetermined intervals and a second information sequence by inserting a second DC control bit different from the first DC control bit into the input information sequence at the predetermined intervals;

a first code converting means for generating a first provisional code sequence by making a code conversion of the first information sequence generated by the information sequence generating means at a conversion ratio of an information word length m to an code word length n;

a second code converting means for generating a second provisional code sequence by making a code conversion of the second information sequence generated by the information sequence generating means at the conversion ratio of the information word length m to the code word length n; and

a selecting means for selecting either the first provisional code sequence generated by the first code converting means or the second provisional code sequence generated by the second code converting means,

the first and second code converting means using a coding rule by which, in case the coding rule is represented by a finite-state code conversion table, code words are assigned to information words so that the two's complement of a sum of coding bits included in the first provisional code sequence is always different from that of a sum of coding bits included in the second provisional code sequence when a first code

state of the first provisional code sequence encoded starting with a predetermined original state, is identical to a second code state of the second provisional code sequence encoded starting with the predetermined original state.

2. The encoder as set forth in claim 1, wherein the first and second cove converting means makes a code conversion with an information word length m of 2 bits and in code conversion units of 2 bits.

3. The encoder as set forth in claim 2, wherein the first and second code converting means uses a coding rule under which the code words are assigned to the information words so that when the first code state is identical the second code state, the two's complement of the sum of coding bits included in the first provisional code sequence is always different from that of the sum of coding bits included in the second provisional code sequence whether the first and second DC control bits are inserted at the first or second bit of the code conversion unit by the information sequence generating means.

4. The encoder as set forth in claim 2, wherein the first and second code converting means uses a coding rule under which the code words are assigned to the information words so that when the first code state is identical to the second code state, the two's complement of the sum of coding bits included in the first provisional code sequence is always different from that of the sum of coding bits included in the second provisional code sequence when the first and second DC control bits are inserted at the first bit of the code conversion unit by the information sequence generating means.

5. The encoder as set forth in claim 2, wherein the first and second code converting means uses a coding rule by which the code words are assigned to the information

words so that when the first code state is identical to the second code state, the two's complement of the sum of coding bits included in the first provisional code sequence is always different from that of the sum of coding bits included in the second provisional code sequence when the first and second DC control bits are inserted at the second bit of the code conversion unit by the information sequence generating means.

6. The encoder as set forth in claim 1, wherein the first and second code converting means is designed to encode information with an information word length m of one block and in units of one block, and the first and second code converting means using a coding rule under which, in case the coding rule is represented by a look-ahead code conversion table, code words are assigned to information words so that the two's complement of a sum of coding bits included in an information sequence is different from that of a sum of coding bits included in a provisional code sequence when the number of blocks is odd while the two's complement of a sum of coding bits included in an information sequence coincides with that of a sum of coding bits included in a provisional code sequence when the number of blocks is even.

7. The encoder as set forth in claim 1, wherein the first and second code converting means is designed to make a code conversion with an information word length of 2 bits taken as one block and in units of one block according to a coding rule in which the information word has a length m of 2 bits, code word has a length n of 3 bits and the maximum run is limited to 7.

8. The encoder as set forth in claim 7, wherein the first and second code converting means uses a coding rule in which, in case the coding rule is represented by a

finite-state code conversion table, the number of states is seven.

9. The encoder as set forth in claim 7, wherein the first and second code converting means is designed to make a code conversion so that the decoded code word constraint length is 3 blocks.

10. The encoder as set forth in claim 1, wherein the first and second code converting means uses a coding rule in which the minimum run is limited to one while the maximum run is limited to seven and the maximum number of minimum runs in sequence of code words is five and, in case the coding rule is represented by a code conversion table, the number of states is eight.

11. The encoder as set forth in claim 1, further comprising a code select signal generating means for calculating the DSV of the first provisional code sequence and that of the second provisional code sequence and generating a code select signal indicative of the provisional code sequence whose DSV is smaller, the selecting means selecting the provisional code sequence whose DSV is smaller according to the code select signal.

12. A coding method comprising the steps of:

generating a first information sequence by inserting a first DC control bit into an input information sequence at predetermined intervals and a second information sequence by inserting a second DC control bit different from the first DC control bit into the input information sequence at the predetermined intervals;

generating a first provisional code sequence by making a code conversion of the first information sequence generated in the information sequence generating step at a conversion ratio of an information word length m to an code word length n;

generating a second provisional code sequence by making a code conversion of the second information sequence generated in the information sequence generating step at the conversion ratio of the information word length m to the code word length n; and

selecting either the first provisional code sequence generated in the first code converting step or the second provisional code sequence generated in the second code converting step,

the first and second code converting steps using a coding rule by which, in case the coding rule is represented by a finite-state code conversion table, code words are assigned to information words so that the two's complement of a sum of coding bits included in the first provisional code sequence is always different from that of a sum of coding bits included in the second provisional code sequence when a first code state of the first provisional code sequence encoded starting with a predetermined original state, is identical to a second code state of the second provisional code sequence encoded starting with the predetermined original state.

13. A recording medium having recorded therein a coding program having a computer convert an m-bit information word continuously into an n-bit code word, the program comprising the steps of:

generating a first information sequence by inserting a first DC control bit into an input information sequence at predetermined intervals and a second information sequence by inserting a second DC control bit different from the first DC control bit into the input information sequence at the predetermined intervals;

generating a first provisional code sequence by making a code conversion of the

first information sequence generated in the information sequence generating step at a conversion ratio of an information word length m to an code word length n;

generating a second provisional code sequence by making a code conversion of the second information sequence generated in the information sequence generating step at the conversion ratio of the information word length m to the code word length n; and

selecting either the first provisional code sequence generated in the first code converting step or the second provisional code sequence generated in the second code converting step,

the first and second code converting steps using a coding rule by which, in case the coding rule is represented by a finite-state code conversion table, code words are assigned to information words so that the two's complement of a sum of coding bits included in the first provisional code sequence is always different from that of a sum of coding bits included in the second provisional code sequence when a first code state of the first provisional code sequence encoded starting with a predetermined original state, is identical to a second code state of the second provisional code sequence encoded starting with the predetermined original state.

14. A coding program for converting an m-bit information word continuously into an n-bit code word, the program comprising the steps of:

generating a first information sequence by inserting a first DC control bit into an input information sequence at predetermined intervals and a second information sequence by inserting a second DC control bit different from the first DC control bit into the input information sequence at the predetermined intervals;

generating a first provisional code sequence by making a code conversion of the first information sequence generated in the information sequence generating step at a conversion ratio of an information word length m to an code word length n;

generating a second provisional code sequence by making a code conversion of the second information sequence generated in the information sequence generating step at the conversion ratio of the information word length m to the code word length n; and

selecting either the first provisional code sequence generated in the first code converting step or the second provisional code sequence generated in the second code converting step,

the first and second code converting steps using a coding rule by which, in case the coding rule is represented by a finite-state code conversion table, code words are assigned to information words so that the two's complement of a sum of coding bits included in the first provisional code sequence is always different from that of a sum of coding bits included in the second provisional code sequence when a first code state of the first provisional code sequence encoded starting with a predetermined original state, is identical to a second code state of the second provisional code sequence encoded starting with the predetermined original state.

15. An encoder comprising:

an input means for receiving m-bit information words;

a coding means for encoding the m-bit information words into n-bit code words according to a coding rule in which the minimum run is limited to one, maximum run is limited to seven and the maximum number of minimum runs of a decoded code

word is three to five; and

an output means for outputting the n-bit code words.

16. The encoder as set forth in claim 15, wherein the coding means uses a coding rule in which, in case the coding rule is represented by a code conversion table, the number of states is eight and the maximum number of minimum runs in sequence is five.

17. The encoder as set forth in claim 15, wherein the coding means encodes the m-bit information words with a decoded code word constraint length of 4 blocks.

18. A coding method comprising the steps of:

receiving an m-bit information word;

encoding the m-bit information word into an n-bit code word under a coding rule in which the minimum run is limited to one, maximum run is limited to seven and the maximum number of minimum runs of a decoded code word is three to five; and

outputting the n-bit code words.

19. A recording medium having recorded therein a coding program, the program comprising the steps of:

receiving an m-bit information word;

encoding the m-bit information word into an n-bit code word under a coding rule in which the minimum run is limited to one, maximum run is limited to seven and the maximum number of minimum runs of a f decoded code word is three to five; and

outputting the n-bit code words.

20. A coding program comprising the steps of:

receiving m-bit information words;

encoding the m-bit information word into an n-bit code word under a coding rule in which the minimum run is limited to one, maximum run is limited to seven and the maximum number of minimum runs of a decoded code word is three to five; and

outputting the n-bit code words.